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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	764	(scan$4 near4 (chain$1 or register$1 or latch$3 or flip-flop$1 or test$3)) and ((isolat$4 or identif$5 or reject$3 or separat$4) near3 (defect$2 or erro$4 or fail$3)) and (correct$3 or modif$5) and (test$3 near2 mode$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 14:09
L2	42	(scan$4 near4 (chain$1 or register$1 or latch$3 or flip-flop$1 or test$3)) and ((isolat$4 or identif$5 or reject$3 or separat$4) near3 (defect$2 or erro$4 or fail$3)) and (correct$3 or modif$5) and (test$3 near2 mode$1) and (lssd or (level adj1 sensitive adj1 scan adj1 design))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 13:16
L3	10	(scan$4 near4 (chain$1 or register$1 or latch$3 or flip-flop$1 or test$3)) same ((isolat$4 or identif$5 or reject$3 or separat$4) near3 (defect$2 or erro$4 or fail$3)) same (correct$3 or modif$5) same (test$3 near2 mode$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 14:11
L4	24	(scan$4 near4 (chain$1 or register$1 or latch$3 or flip-flop$1 or test$3)) same ((isolat$4 or identif$5 or reject$3 or separat$4) near3 (defect$2 or erro$4 or fail$3)) same (test$3 near2 mode$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 14:11
L5	542	(scan$4 near4 (chain$1 or register$1 or latch$3 or flip-flop$1 or test$3)) and ((isolat$4 or identif$5 or reject$3 or separat$4) near3 (defect$2 or erro$4 or fail$3)) and (test adj2 mode$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 14:12
L6	542	((scan$4 near4 (chain$1 or register$1 or latch$3 or flip-flop$1 or test$3)) and (test adj2 mode$1)) and ((isolat$4 or identif$5 or reject$3 or separat$4) near3 (defect$2 or erro$4 or fail$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 14:13

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L7	285	((scan$4 near4 (chain$1 or register$1 or latch$3 or flip-flop$1 or test$3)) same (test adj2 mode$1)) and ((isolat$4 or identif$5 or reject$3 or separat$4) near3 (defect$2 or erro$4 or fail$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 14:13
L8	168	((scan$4 near4 (chain$1 or register$1 or latch$3 or flip-flop$1 or test$3)) same (test adj2 mode$1)) and ((isolat$4 or separat$4) near3 (defect$2 or erro$4 or fail$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 14:14
L9	31	((scan$4 near4 (chain$1 or register$1 or latch$3 or flip-flop$1 or test$3)) same (test adj2 modes)) and ((isolat$4 or separat$4) near3 (defect$2 or erro$4 or fail$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 14:23
L10	697	(first adj2 (test or scan or capture) adj2 mode) and (second adj2 (test or scan or capture) adj2 mode)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 14:25
L12	8	(first adj2 (test or scan or capture) adj2 mode) same (second adj2 (test or scan or capture) adj2 mode) same modif$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 14:26
L13	120	((first adj2 (test or scan or capture) adj2 mode) same (second adj2 (test or scan or capture) adj2 mode)) and modif$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/11/09 14:27

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Inventor Name Search Result

Your Search was:

Last Name = HUISMAN
First Name = LEENDERT

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09524254	6931580	150	03/13/2000	RAPID FAIL ANAYSIS OF EMBEDDED OBJECTS	HUISMAN, LEENDERT M.
09682456	6675323	150	09/05/2001	INCREMENTAL FAULT DICTIONARY	HUISMAN, LEENDERT M.
09827425	6721914	150	04/06/2001	DIAGNOSIS OF COMBINATIONAL LOGIC CIRCUIT FAILURES	HUISMAN, LEENDERT M.
09927011	6901542	150	08/09/2001	INTERNAL CACHE FOR ON CHIP TEST DATA STORAGE	HUISMAN, LEENDERT M.
09930355	6671644	150	08/15/2001	USING CLOCK GATING OR SIGNAL GATING TO PARTITION A DEVICE FOR FAULT ISOLATION AND DIAGNOSTIC DATA COLLECTION	HUISMAN, LEENDERT M.
10191212	6880136	150	07/09/2002	METHOD TO DETECT SYSTEMATIC DEFECTS IN VLSI MANUFACTURING	HUISMAN, LEENDERT M.
10604179	6954916	150	06/30/2003	METHODOLOGY FOR FIXING QCRIT AT DESIGN TIMING IMPACT	HUISMAN, LEENDERT M.
10697365	6865501	150	10/30/2003	USING CLOCK GATING OR SIGNAL GATING TO PARTITION A DEVICE FOR FAULT ISOLATION AND DIAGNOSTIC DATA COLLECTION	HUISMAN, LEENDERT M.
10707373	Not Issued	41	12/09/2003	SCAN CHAIN DIAGNOSTICS USING LOGIC PATHS	HUISMAN, LEENDERT M.
10707957	7139950	150	01/28/2004	SEGMENTED SCAN CHAINS WITH DYNAMIC RECONFIGURATIONS	HUISMAN, LEENDERT M.
10708380	Not Issued	30	02/27/2004	METHODS AND APPARATUS FOR DEFECT ISOLATION	HUISMAN, LEENDERT M.

10709672	Not Issued	30	05/21/2004	LEARNING BASED LOGIC DIAGNOSIS	HUISMAN, LEENDERT M.
10710642	Not Issued	93	07/27/2004	DESIGNING SCAN CHAINS WITH SPECIFIC PARAMETER SENSITIVITIES TO IDENTIFY PROCESS DEFECTS	HUISMAN, LEENDERT M.
10710879	7089514	150	08/10/2004	DEFECT DIAGNOSIS FOR SEMICONDUCTOR INTEGRATED CIRCUITS	HUISMAN, LEENDERT M.
10711765	Not Issued	41	10/04/2004	INSPECTION METHODS AND STRUCTURES FOR VISUALIZING AND/OR DETECTING SPECIFIC CHIP STRUCTURES	HUISMAN, LEENDERT M.
11006274	Not Issued	41	12/07/2004	Using clock gating or signal gating to partition a device for fault isolation and diagnostic data collection	HUISMAN, LEENDERT M.
06862950	4726023	150	05/14/1986	DETERMINATION OF TESTABILITY OF COMBINED LOGIC END MEMORY BY IGNORING MEMORY	HUISMAN, LEENDERT M.
07900706	5297151	250	06/17/1992	ADJUSTABLE WEIGHTED RANDOM TEST PATTERN GENERATOR FOR LOGIC CIRCUITS	HUISMAN, LEENDERT M.
08811605	6519725	150	03/04/1997	DIAGNOSIS OF RAMS USING FUNCTIONAL PATTERNS	HUISMAN, LEENDERT M.
09032567	6170078	150	02/27/1998	FAULT SIMULATION USING DYNAMICALLY ALTERABLE BEHAVIORAL MODELS	HUISMAN, LEENDERT M.
09379772	6785413	150	08/24/1999	RAPID DEFECT ANALYSIS BY PLACEMENT OF TESTER FAIL DATA	HUISMAN, LEENDERT M.
09026286	6125461	150	02/19/1998	METHOD FOR IDENTIFYING LONG PATHS IN INTEGRATED CIRCUITS	HUISMAN, LEENDERT MARINUS

Inventor Search Completed: No Records to Display.

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